

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-4 (canceled)

5. (currently amended) ~~The microelectronic device of claim 1, wherein:~~

A microelectronic device comprising:

a die having an active surface fixed within an opening in a package core by an encapsulation material between said die and said package core;

a metallization layer built up upon said active surface of said die and said package core; and

a grid array interposer unit having a first surface laminated to said metallization layer, said grid array interposer unit having an array of electrical contacts on a second surface thereof for connection to an external circuit board, wherein said grid array interposer unit includes an opening that exposes a first portion of said metallization layer, said microelectronic device further comprising at least one de-coupling capacitor connected to said first portion of said metallization layer to provide de-coupling for circuitry within said die.

6. (canceled)

7. (currently amended) The microelectronic device of claim 5 [[1]], wherein:  
said package core is formed from a dielectric board material having a metallic cladding on at least one surface thereof.
8. (original) The microelectronic device of claim 7, wherein:  
said metallic cladding is conductively coupled to ground during operation of said device to provide a ground plane for at least one transmission structure within said metallization layer.
9. (original) The microelectronic device of claim 7, wherein:  
said metallic cladding is conductively coupled to a power source during device operation to form a power plane.
10. (original) The microelectronic device of claim 7, wherein:  
said metallization layer includes at least one ground pad that is conductively coupled to said metallic cladding on said package core through one or more via connections.
11. (currently amended) The microelectronic device of claim 5 [[1]], wherein:  
said active surface includes a plurality of power bars and a plurality of ground bars, each of said plurality of power bars being conductively coupled to multiple power bond pads of said die and each of said plurality of ground bars being conductively coupled to multiple ground bond pads of said die.

12. (previously presented) The microelectronic device of claim 11, wherein:  
said plurality of power bars and said plurality of ground bars are interleaved within a central region of said active surface of said die.
13. (previously presented) The microelectronic device of claim 11, wherein:  
said die includes a plurality of signal contact pads distributed within a peripheral region of said active surface.
14. (currently amended) The microelectronic device of claim 5 [[1]], wherein:  
said metallization layer includes at least one power landing pad situated over said die, said at least one power landing pad being conductively coupled to multiple power bond pads on said die through corresponding via connections.
15. (original) The microelectronic device of claim 14, wherein:  
said metallization layer includes at least one ground landing pad situated over said die, said at least one ground landing pad being conductively coupled to multiple ground bond pads on said die through corresponding via connections.
16. (currently amended) The microelectronic device of claim 5 [[1]], wherein:  
said metallization layer includes at least one power landing pad situated over said package core, said at least one power landing pad being conductively coupled to

multiple power bond pads on said die through a trace portion extending over said die and a plurality of via connections.

17. (currently amended) The microelectronic device of claim 5 [[1]], wherein:

said metallization layer includes at least one signal landing pad situated over said package core, said at least one signal landing pad being conductively coupled to a signal bond pad on said die through a path including a transmission line segment.

18. (currently amended) The microelectronic device of claim 5 [[1]], wherein:

said microelectronic device includes a single metallization layer between said die and said grid array interposer unit.

19 – 23 (canceled)

24. (currently amended) An electrical system comprising:

a microelectronic device having:

a die/core assembly including a die fixed within an opening in a package core by an encapsulation material between said die and said package core, said die/core assembly having a first surface including an active surface of said die;

a metallization layer built up over said first surface of said die/core assembly, said metallization layer having a first metallization portion over said die and a second metallization portion over said package core; and

a grid array interposer unit laminated to said metallization layer, said grid array interposer unit having a first array of electrical contacts on a surface thereof; and

at least one capacitor conductively coupled to an exposed portion of said metallization layer to provide de-coupling for circuitry within said microelectronic die; and

a circuit board having a second array of electrical contacts, said grid array interposer unit being coupled to said circuit board so that contacts within said first array of electrical contacts are conductively coupled to corresponding contacts within said second array of electrical contacts.

25. (previously presented) The electrical system claimed in claim 24, wherein:  
said circuit board is a computer motherboard.

26. (previously presented) The electrical system of claim 25, wherein:  
said first array of electrical contacts includes a plurality of pins.

27. (previously presented) The electrical system of claim 25, wherein:  
said first array of electrical contacts includes a plurality of solder balls.

28. (previously presented) A microelectronic device comprising:  
a die/core assembly having a microelectronic die fixed within an opening in a package core by an encapsulation material between said die and said package core,

said die/core assembly having including a first surface including an active surface of said die;

a metallization layer built up over said first surface of said die/core assembly, said metallization layer having a first metallization portion over said die and a second metallization portion over said package core;

a grid array interposer unit laminated to said metallization layer; and

at least one capacitor conductively coupled to an exposed portion of said metallization layer to provide de-coupling for circuitry within said microelectronic die.

29. (original) The microelectronic device of claim 28, wherein:

said metallization layer includes at least one power landing pad situated over said microelectronic die that is conductively coupled to multiple power bond pads on said die and also to a corresponding power contact on said grid array interposer unit.

30. (original) The microelectronic device of claim 28, wherein:

said metallization layer includes at least one power landing pad situated over said package core that is conductively coupled to multiple power bond pads on said die and also to a corresponding power contact on said grid array interposer unit.

31 – 33 (canceled)

34. (currently amended) ~~The microelectronic device of claim 32, wherein:~~

A microelectronic device comprising:

a die having an active surface fixed within an opening in a package core by an encapsulation material between said die and said package core;

a metallization layer built up upon said active surface of said die and said package core, wherein said metallization layer includes a first metallization portion located over said die and a second metallization portion located over said package core; and

a grid array interposer unit having a first surface laminated to said metallization layer, said grid array interposer unit having an array of electrical contacts on a second surface thereof for connection to an external circuit board, and wherein said grid array interposer unit has a thickness between said first and second surfaces that is no greater than 0.5 millimeters and said grid array interposer unit includes an opening that exposes a first portion of said metallization layer, said microelectronic device further comprising at least one de-coupling capacitor connected to said first portion of said metallization layer to provide de-coupling for circuitry within said die.

35. (currently amended) The microelectronic device of claim 34 ~~[[32]]~~, wherein:

said metallization layer includes at least one ground pad that is conductively coupled to said metallic cladding on said package core through one or more via connections.

36. (canceled)

37. (currently amended) ~~The microelectronic device of claim 36, further comprising:~~

A microelectronic device comprising:

a die having an active surface fixed within a package core;

a metallization layer adjacent to said active surface of said die and said package core;

a grid array interposer unit having a first surface laminated to said metallization layer, said grid array interposer unit having an array of electrical contacts on a second surface thereof for connection to an external circuit board; and

a dielectric layer between said metallization layer and said active surface of said die and said package core.

38. (previously presented) The microelectronic device of claim 37, wherein:

said metallization layer is conductively coupled to said active surface of said die through via connections in said dielectric layer.

39. (canceled)

40. (currently amended) The microelectronic device of claim 37 [[36]], wherein:

said metallization layer includes at least one I/O landing pad to said active surface of said die by a transmission line segment.

41. (previously presented) A microelectronic device comprising:

a die/core assembly including a die fixed within a package core, said die/core assembly having a continuous surface;

a metallization layer built up upon said continuous surface; and

a grid array interposer unit having a first surface laminated to said metallization layer, said grid array interposer unit having an array of electrical contacts on a second surface thereof for connection to an external circuit board.

42. (previously presented) The microelectronic device of claim 41, wherein:

said die is fixed within said package core by an encapsulation material between said die and said package core.

43 ~~[[45]]~~. (currently amended) The microelectronic device of claim 42, wherein:

said package core includes an opening that extends through said package core.

44. (previously presented) The microelectronic device of claim 41, wherein:

said continuous surface comprises a dielectric layer.

45. (previously presented) The microelectronic device of claim 43, wherein:

said metallization layer is conductively coupled to said active surface of said die through via connections in said dielectric layer.

46. (new) The microelectronic device of claim 41, wherein:

said package core comprises a metallic cladding on at least one surface thereof.

47. (new) The microelectronic device of claim 46, wherein:

said metallic cladding is conductively coupled to ground during device operation to provide a ground plane.

48. (new) The microelectronic device of claim 46, wherein:

said metallic cladding is conductively coupled to a power source during device operation to provide a power plane.

49. (new) The microelectronic device of claim 41, wherein:

said metallization layer includes a power landing pad situated over said die, said power landing pad being conductively coupled to a power bond pad on said die through a via connection.

50. (new) The microelectronic device of claim 41, wherein:

said metallization layer includes a ground landing pad situated over said die, said ground landing pad being conductively coupled to a ground bond pad on said die through a via connection.

51. (new) The microelectronic device of claim 41, wherein:

said metallization layer includes a signal landing pad situated over said package core, said signal landing pad being conductively coupled to a signal bond pad on said die through a transmission line segment.

52. (new) The microelectronic device of claim 41, further comprising:  
a de-coupling capacitor connected to said second surface of said grid array  
interposer unit to provide de-coupling for circuitry within said die.

53. (new) The microelectronic device of claim 41, further comprising:  
a circuit board having a second array of electrical contacts, wherein said grid  
array interposer unit is conductively coupled to said circuit board.